

March. 14, 2019

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| Delay on: D6.5 | Optimised interconnection process |
| Delivery Date in Annex 1: | M42 |
| Expected Delivery Date: | M49 |

The focus of the HV/HR-CMOS effort shifted from hybrid devices to monolithic ones, which do not require a complicated interconnection technique as bump-bonding or the precise alignment needed in AC-coupled assemblies. However, during the hybridization activities of WP6 substantial progress was made in the fabrication of DC and AC coupled devices. An interesting development is the investigation of the wafer packaging technique, that allows to reduce production costs and recover devices during the fabrication process. This technique is still being investigated, and the deliverable date has been moved to M49 to be able to include the latest developments in this area.