



March. 13, 2019

<b>Delay on: MS 97</b>	Test report of deliverable D4.3
<b>Delivery Date in Annex 1:</b>	M46
<b>Expected Delivery Date:</b>	M58

MS97 concerns test results on Through-Silicon Via (TSV) interconnects in RD53A 65 nm CMOS wafers. From previous experience, we know that TSV etching is a complex process that takes several months to complete its various steps (e.g. silicon etching, via filling, backside metallization) Also, wafer testing requires an adequate time to fully understand the behavior of integrated circuits after the TSV process. So, since deliverable D4.3 was moved to M54 after the 1-year project extension, it is desirable to postpone MS97 to February 2020 (M58), so that we are able to complete the characterization of 65 nm wafers with TSVs.